ABSTRACT OF THE DISCLOSURE

A flash memory comprises a memory sector, a command interface, a first signal buffer, a control signal generation circuit, a control signal generation circuit, a data input buffer, an error correction circuit, an address buffer, an address signal generation circuit, a plurality of data memory circuits, and write means. The command interface receives a write data input instruction from an external device to generate a write data input instruction signal, and receives a write instruction from the external device to generate a write instruction signal. The error correction circuit is activated by the write data input instruction signal to receive the write data in synchronization with the write enable signal, and is activated by the write instruction signal to generate a check data for an error correction in synchronization with the control signal. With this configuration, processing to generate the check data for the error correction with the internal error correction circuit and processing to input the check data to the write circuit, etc. can be automatically performed in the flash memory even in the period when the external control signal is not input.